FIGURE 1

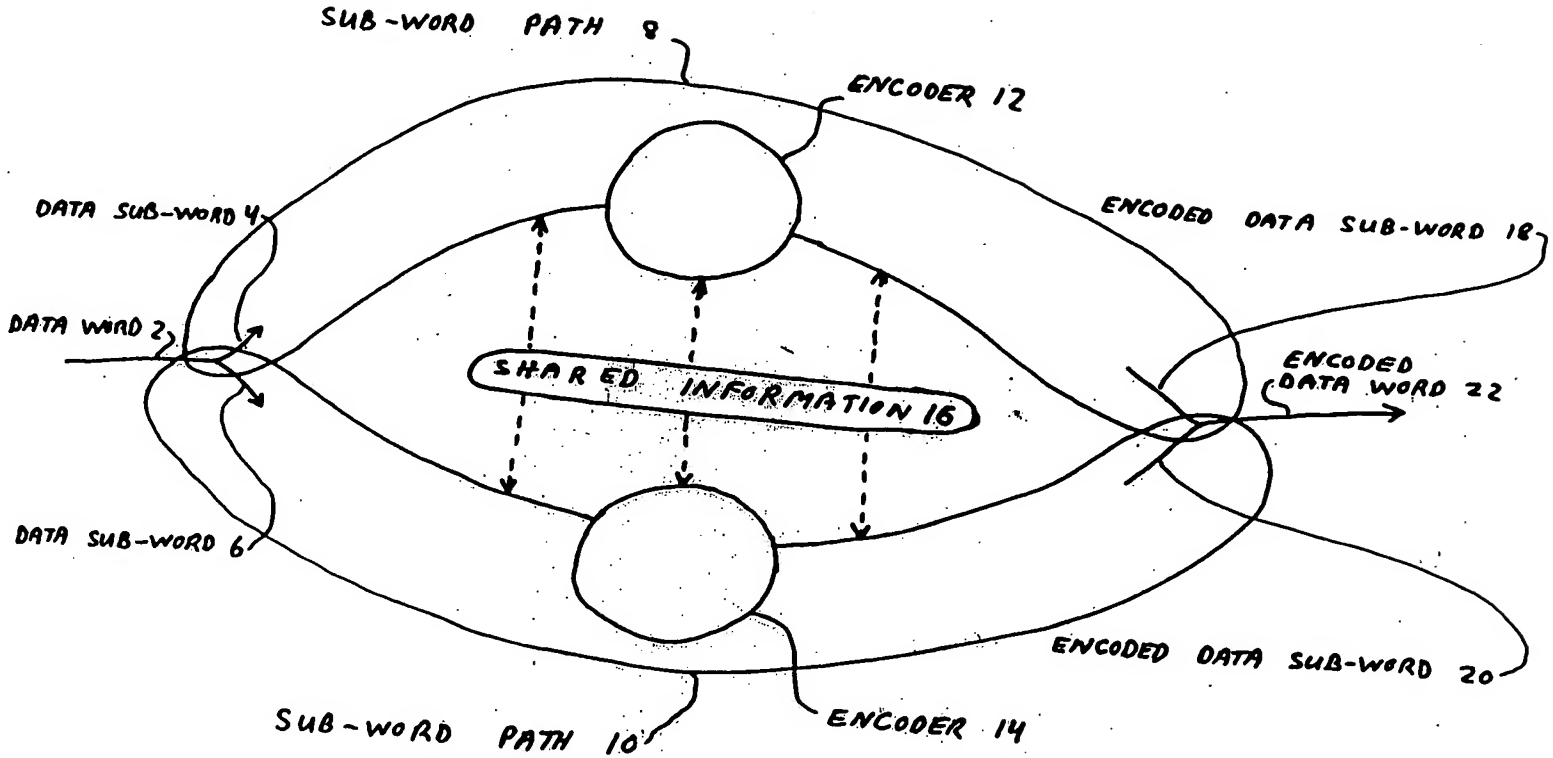
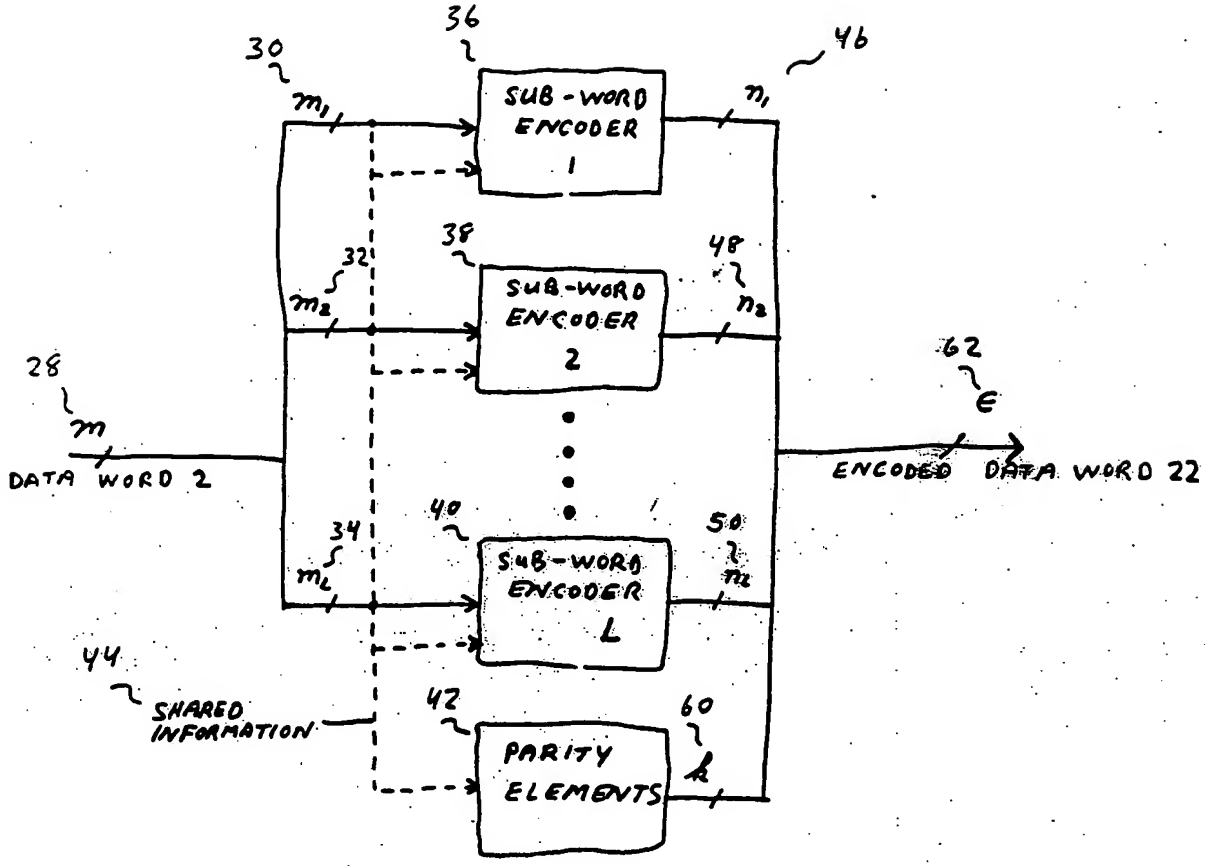

SUB-WORD PATH 8
ENCODER 12
DATA SUB-WORD 4
ENCODED DATA SUB-WORD 18
DATA WORD 2
SHARED INFORMATION 16
ENCODED DATA WORD 22
DATA SUB-WORD 6
ENCODED DATA SUB-WORD 20
SUB-WORD PATH 10
ENCODER 14

FIG 2



64

$$\epsilon = (\quad n_1) + (\quad n_2) + \ldots . (\quad n_L) + k$$

and $n_1 > m_1,\ n_2 > m_2, \ldots . n_L > m_L$

FIGURE 3

66

NUMBER OF ENCODED LINES (n)	P=0	P=1	P=2	P=3	P=4	P=5	P=6	P=7	P=8	P=9	P=10
n=1	1.	1.									
n=2	1.	2.	1.								
n=3	1.	3.	3.	1.							
n=4	1.	4.	6.	4.	1.						
n=5	1.	5.	10.	10.	5.	1.					
n=6	1.	6.	15.	20.	15.	6.	1.				
n=7	1.	7.	21.	35.	35.	21.	7.	1.			
n=8	1.	8.	28.	56.	70.	56.	28.	8.	1.		
n=9	1.	9.	36.	84.	126.	126.	84.	36.	9.	1.	
n=10	1.	10.	45.	120.	210.	252.	210.	120.	45.	10.	1.

NUMBER OF ONES (P) IN AN ENCODED WORD

FIGURE 4

68

ENCODED WORD Length	Code States	INPUT WORD LENGTH	Extra Lines
3	2	1	2
4	6	2	2
5	10	3	2
6	20	4	2
7	35	5	2
8	70	6	2
9	126	6	3
10	252	7	3
11	462	8	3
12	924	9	3
13	1716	10	3
14	3432	11	3
15	6435	12	3
16	12870	13	3
17	24310	14	3
18	48620	15	3
19	92378	16	3
20	184756	17	3
21	352716	18	3

FIG 5

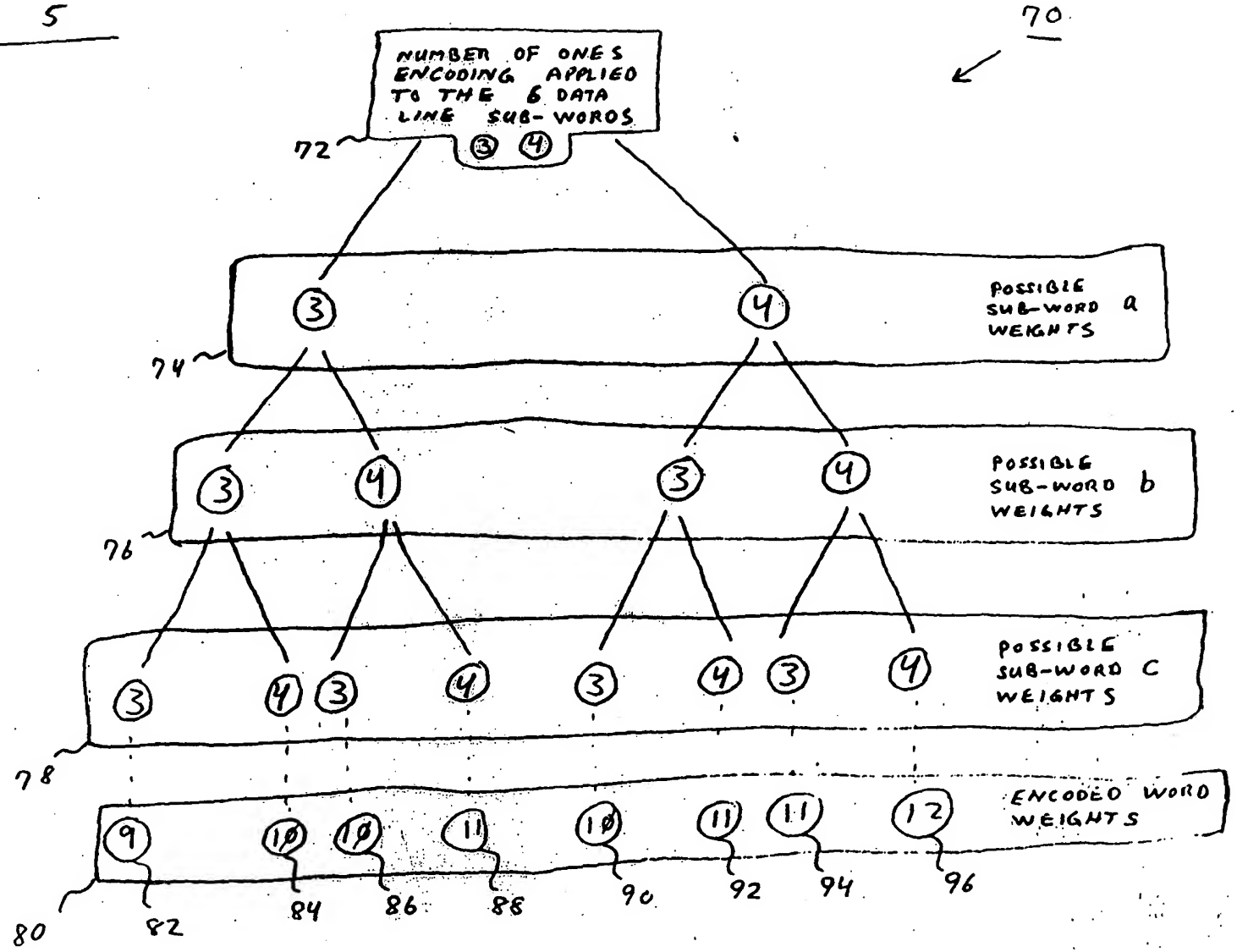

70
NUMBER OF ONES ENCODING APPLIED TO THE 6 DATA LINE SUB-WORDS
3 4
72
3
4
POSSIBLE SUB-WORD a WEIGHTS
74
3
4
3
4
POSSIBLE SUB-WORD b WEIGHTS
76
3
4 3
4
3
4 3
4
POSSIBLE SUB-WORD C WEIGHTS
78
9
10
10
11
10
11
11
12
ENCODED WORD WEIGHTS
80
82
84
86
88
90
92
94
96

FIG 6

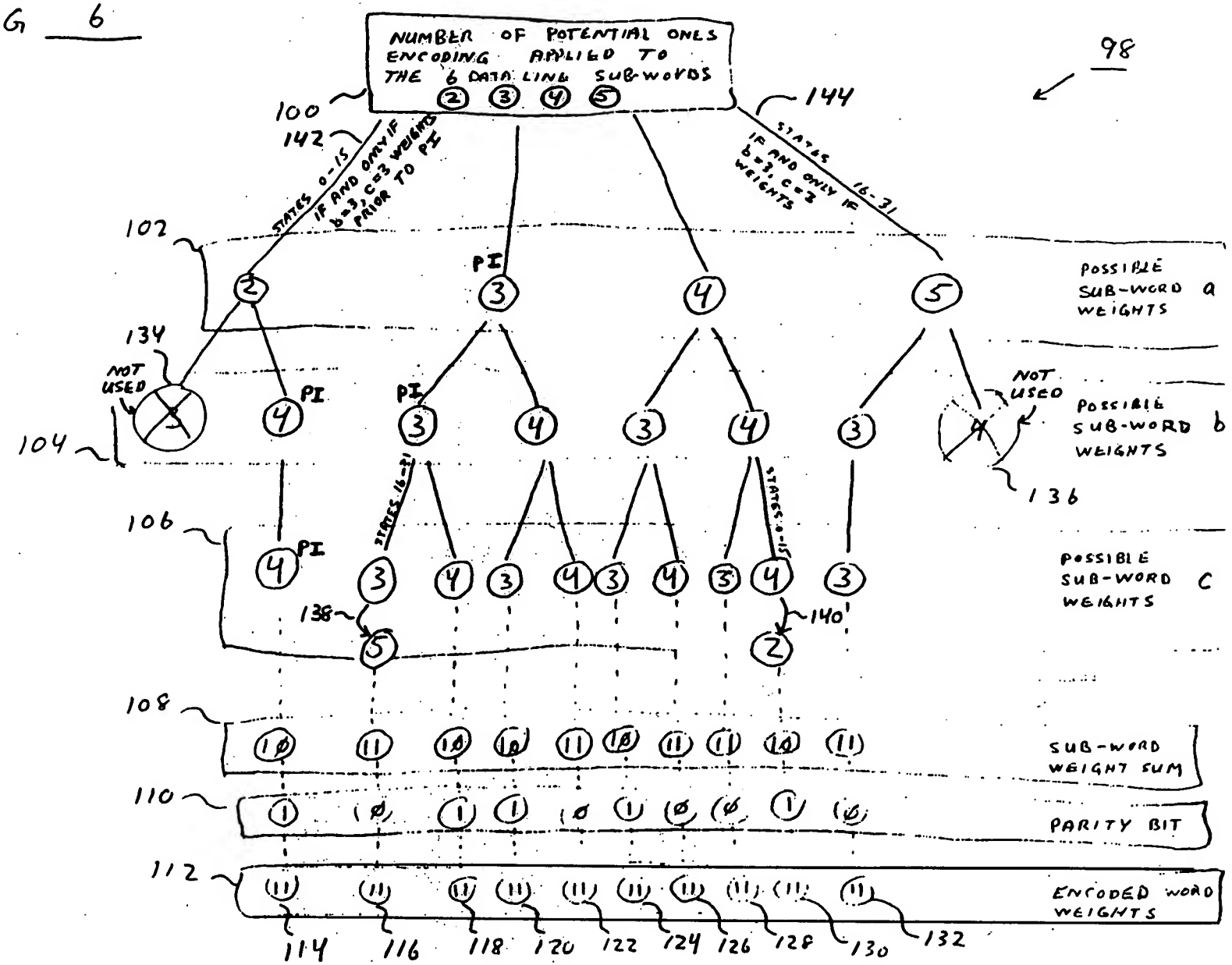

NUMBER OF POTENTIAL ONES ENCODING APPLIED TO THE 6 DATA LINE SUB-WORDS
2 3 4 5
98
100
142
144
STATES 0-15 IF AND ONLY IF b=3, c=3 WEIGHTS PRIOR TO PI
STATES 16-31 IF AND ONLY IF b=3, c=3 WEIGHTS
102
PI
POSSIBLE SUB-WORD a WEIGHTS
134
NOT USED
PI
PI
NOT USED
POSSIBLE SUB-WORD b WEIGHTS
136
104
106
PI
STATES 16-31
STATES 0-15
POSSIBLE SUB-WORD c WEIGHTS
138
140
108
SUB-WORD WEIGHT SUM
110
PARITY BIT
112
ENCODED WORD WEIGHTS
114
116
118
120
122
124
126
128
130
132

FIGURE 7

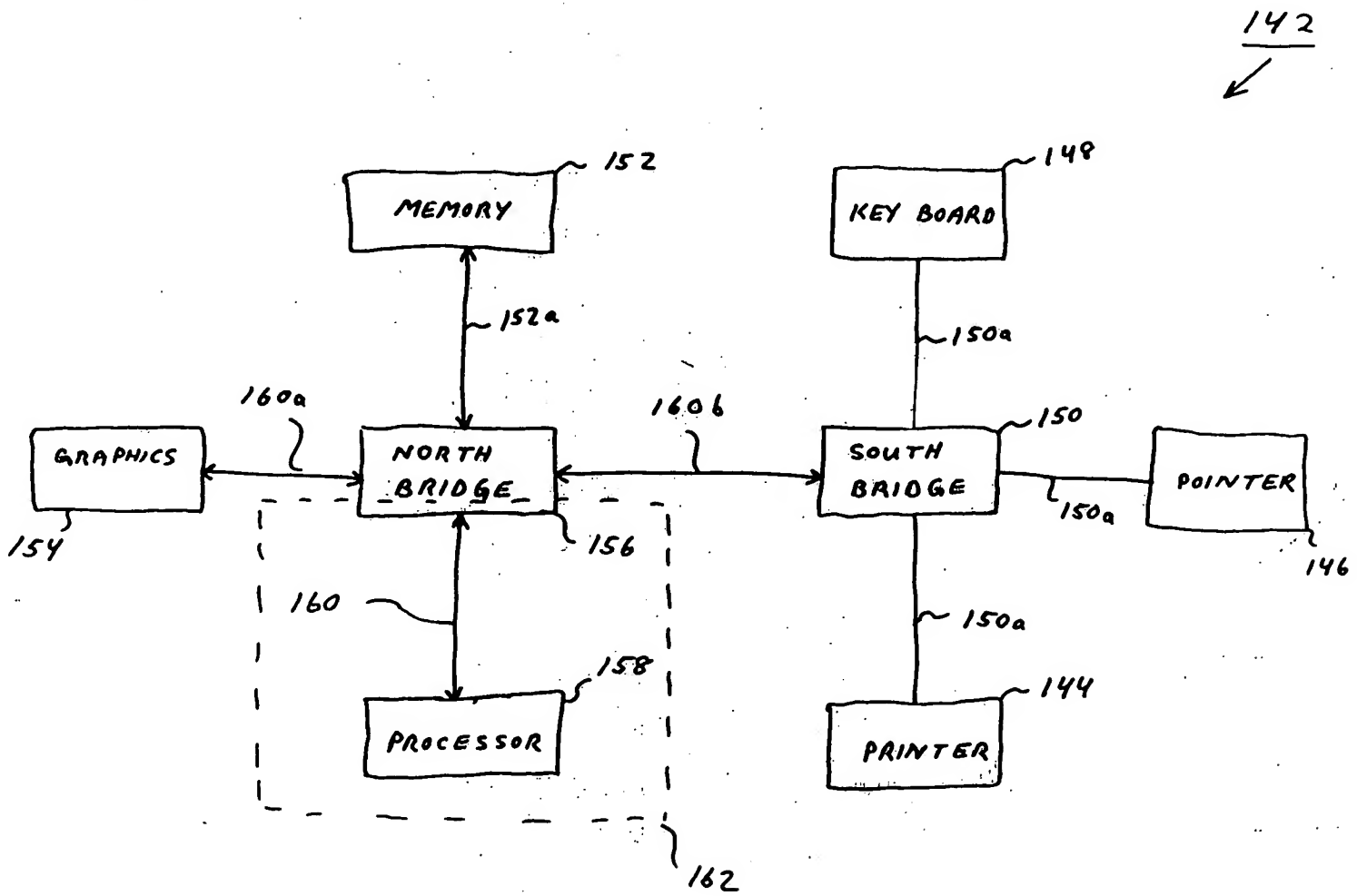

142
MEMORY
152
KEY BOARD
148
152a
150a
160a
160b
GRAPHICS
NORTH BRIDGE
SOUTH BRIDGE
150
POINTER
154
156
150a
146
160
150a
158
144
PROCESSOR
PRINTER
162

FIGURE 8

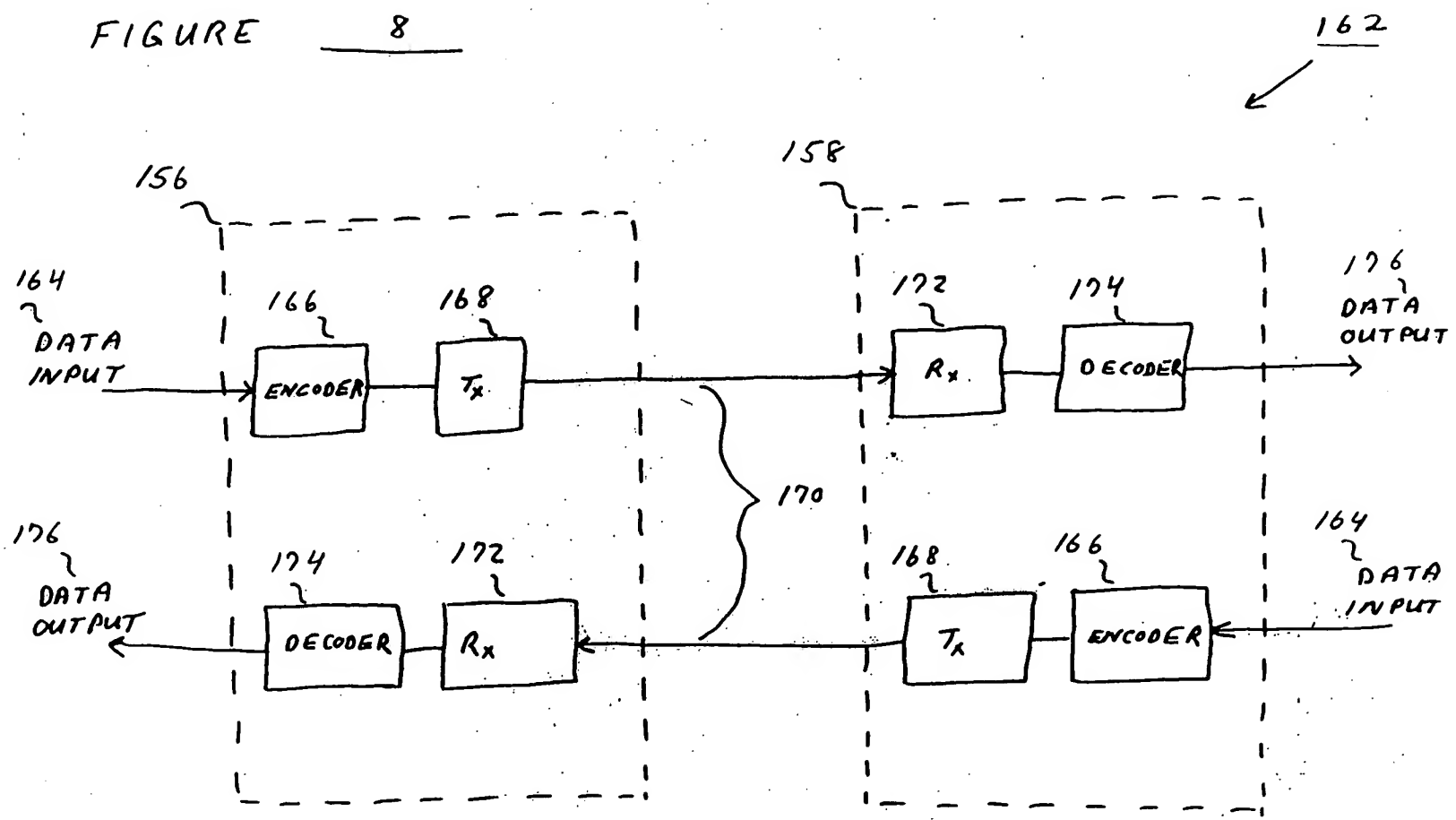

162
156
158
164
DATA INPUT
166
ENCODER
168
T_x
172
R_x
174
DECODER
176
DATA OUTPUT
170
176
DATA OUTPUT
174
DECODER
172
R_x
168
T_x
166
ENCODER
164
DATA INPUT

FIGURE 9

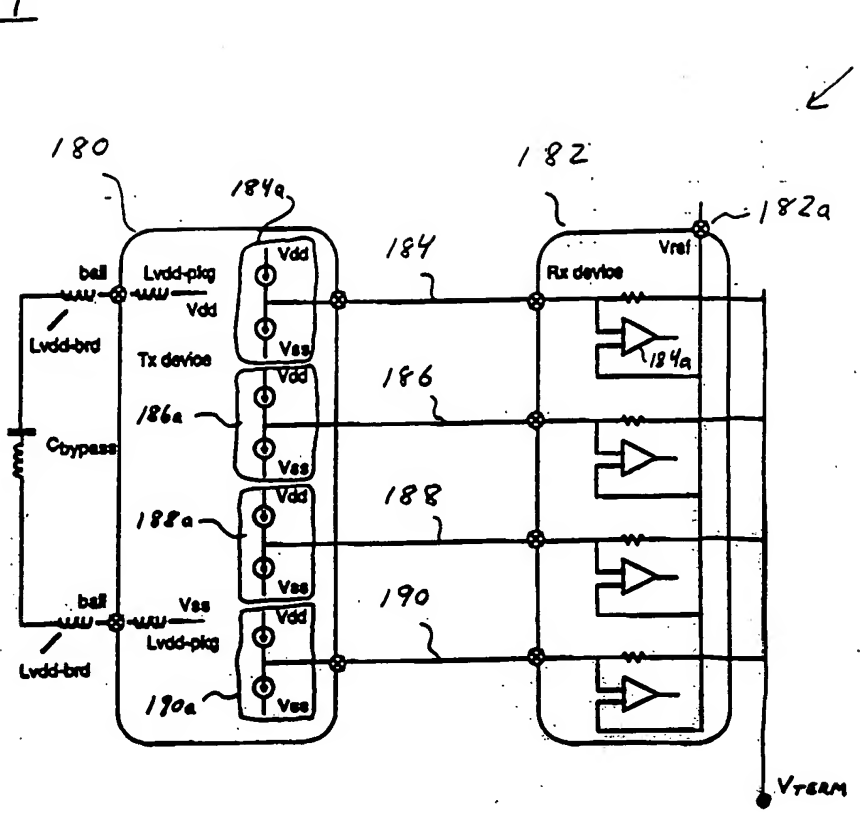


FIGURE 10

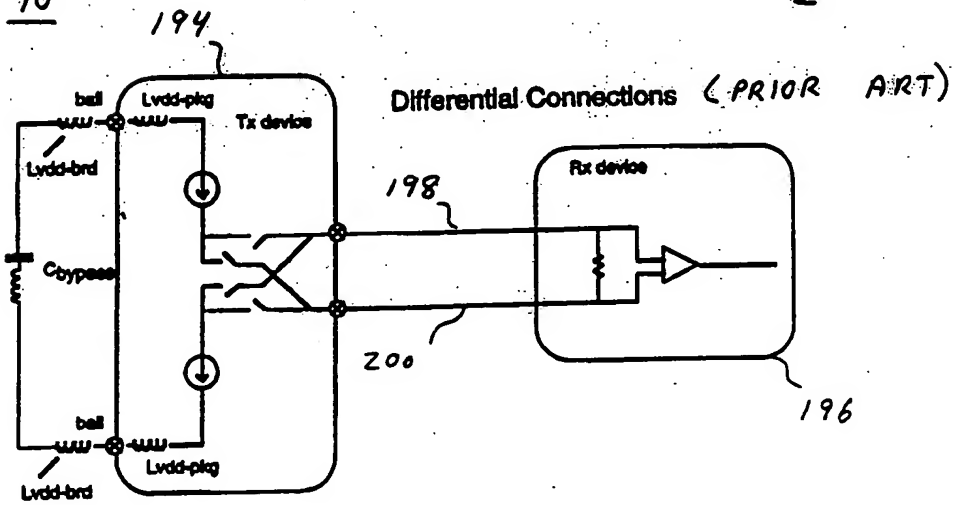


FIG 11

166

Top-level block diagram for the encoder

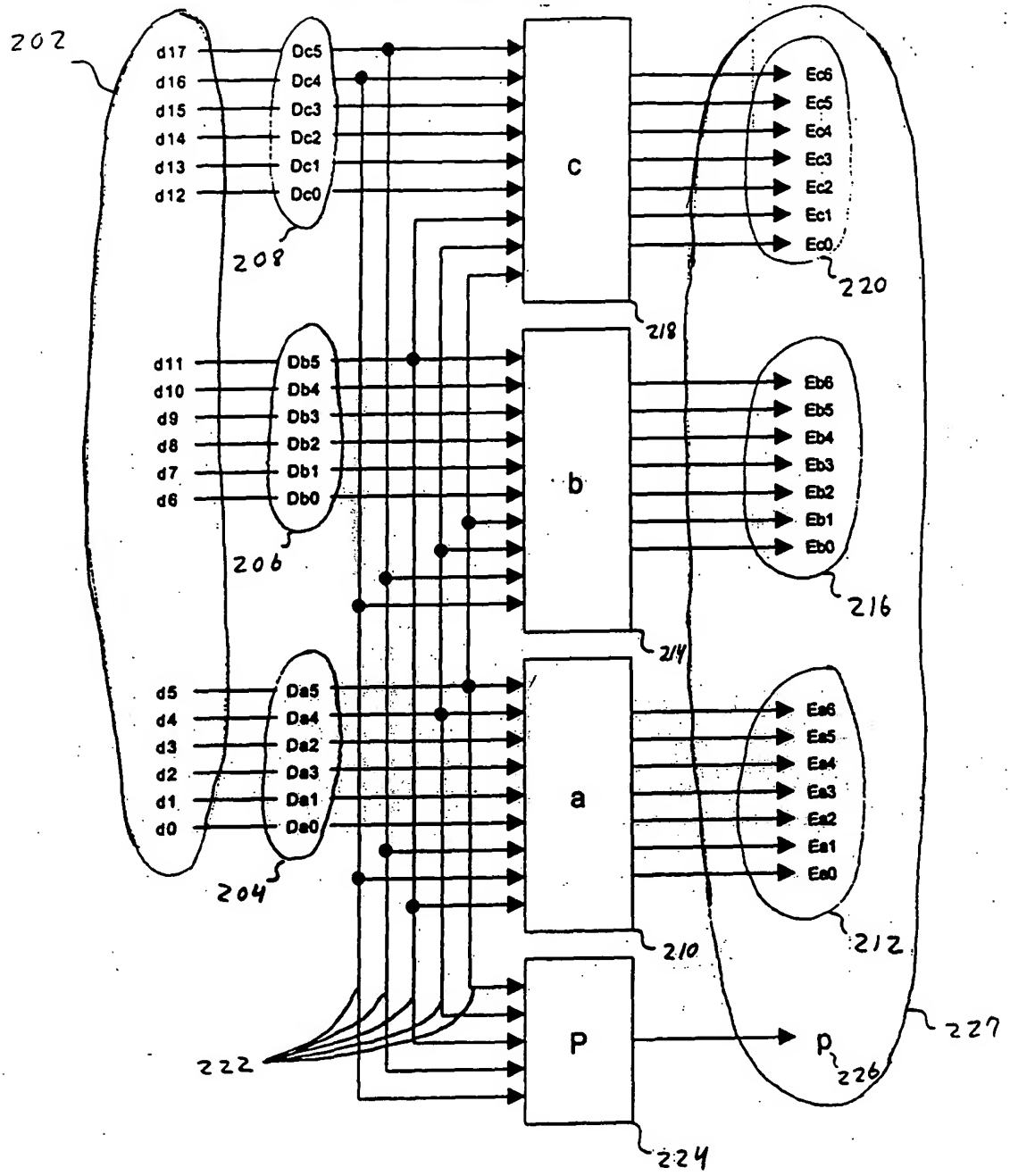


FIG 12

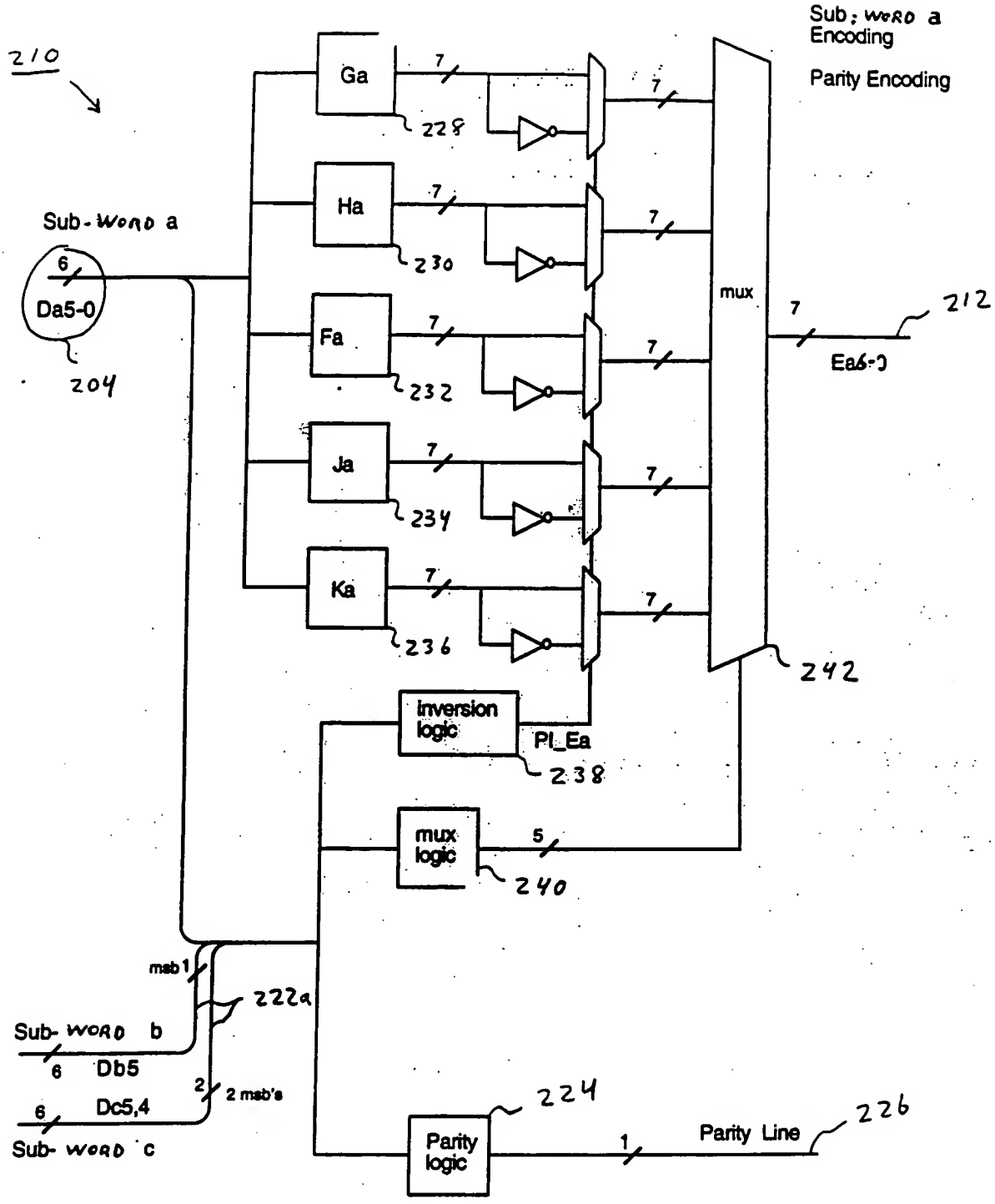
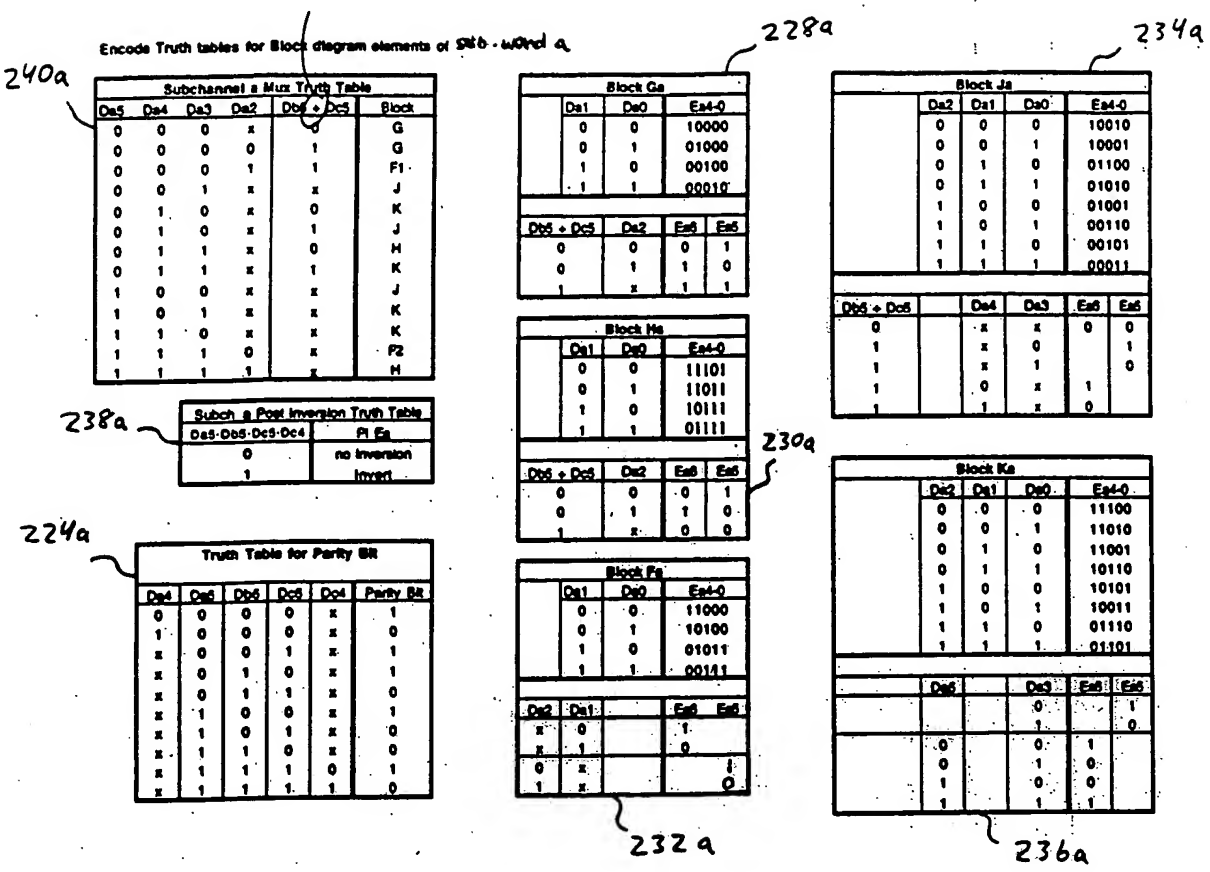

210
Sub-word a
6
Da5-0
204
Ga
Ha
Fa
Ja
Ka
7
228
230
232
234
236
Sub; word a Encoding
Parity Encoding
mux
7
212
Ea6-0
242
inversion logic
Pl_Ea
238
mux logic
5
240
msb 1
222a
Sub-word b
6
Db5
2
2 msb's
6
Dc5,4
Sub-word c
224
Parity logic
1
Parity Line
226

FIG 13



Subchannel a Mux Truth Table

Da5	Da4	Da3	Da2	Db5 + Dc5	Block
0	0	0	x	0	G
0	0	0	0	1	G
0	0	0	1	1	F1
0	0	1	x	x	J
0	1	0	x	0	K
0	1	0	x	1	J
0	1	1	x	0	H
0	1	1	x	1	K
1	0	0	x	x	J
1	0	1	x	x	K
1	1	0	x	x	K
1	1	1	0	x	F2
1	1	1	1	x	H

Subch a Post Inversion Truth Table

Da5·Db5·Dc5·Dc4	Pl Ea
0	no inversion
1	Invert

Truth Table for Parity Bit

Da4	Da5	Db5	Dc5	Dc4	Parity Bit
0	0	0	0	x	1
1	0	0	0	x	0
x	0	0	1	x	1
x	0	1	0	x	1
x	0	1	1	x	0
x	1	0	0	x	1
x	1	0	1	x	0
x	1	1	0	x	0
x	1	1	1	0	1
x	1	1	1	1	0

Block Ga

Da1	Da0	Ea4-0
0	0	10000
0	1	01000
1	0	00100
1	1	00010

Db5 + Dc5	Da2	Ea6	Ea5
0	0	0	1
0	1	1	0
1	x	1	1

Block Ha

Da1	Da0	Ea4-0
0	0	11101
0	1	11011
1	0	10111
1	1	01111

Db5 + Dc5	Da2	Ea6	Ea5
0	0	0	1
0	1	1	0
1	x	0	0

Block Fa

Da1	Da0	Ea4-0
0	0	11000
0	1	10100
1	0	01011
1	1	00111

Da2	Da1		Ea6	Ea5
x	0		1	
x	1		0	
0	x			1
1	x			0

Block Ja

Da2	Da1	Da0	Ea4-0
0	0	0	10010
0	0	1	10001
0	1	0	01100
0	1	1	01010
1	0	0	01001
1	0	1	00110
1	1	0	00101
1	1	1	00011

Db5 + Dc5	Da4	Da3	Ea6	Ea5
0	x	x	0	0
1	x	0		1
1	x	1		0
1	0	x	1	
1	1	x	0	

Block Ka

Da2	Da1	Da0	Ea4-0
0	0	0	11100
0	0	1	11010
0	1	0	11001
0	1	1	10110
1	0	0	10101
1	0	1	10011
1	1	0	01110
1	1	1	01101

	Da5		Da3	Ea6	Ea5
			0		1
			1		0
	0		0	1	
	0		1	0	
	1		0	0	
	1		1	1	

FIG 14

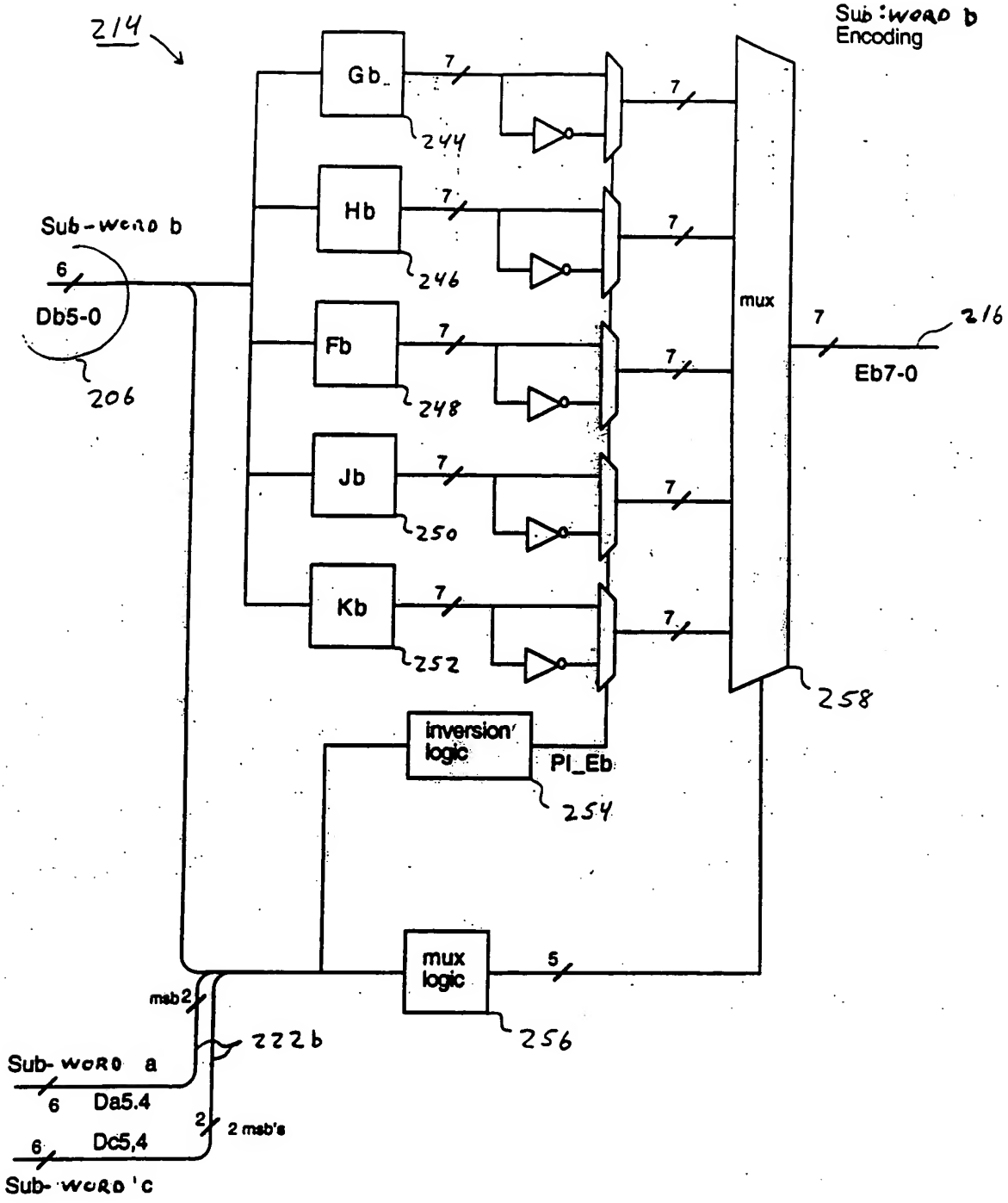

214
Sub-word b Encoding
Gb
Hb
Fb
Jb
Kb
244
246
248
250
252
7
Sub-word b
6
Db5-0
206
mux
7
216
Eb7-0
258
inversion logic
Pl_Eb
254
mux logic
5
256
mab2
222b
Sub-word a
6
Da5.4
2
2 mab's
6
Dc5,4
Sub-word 'c

FIG 15

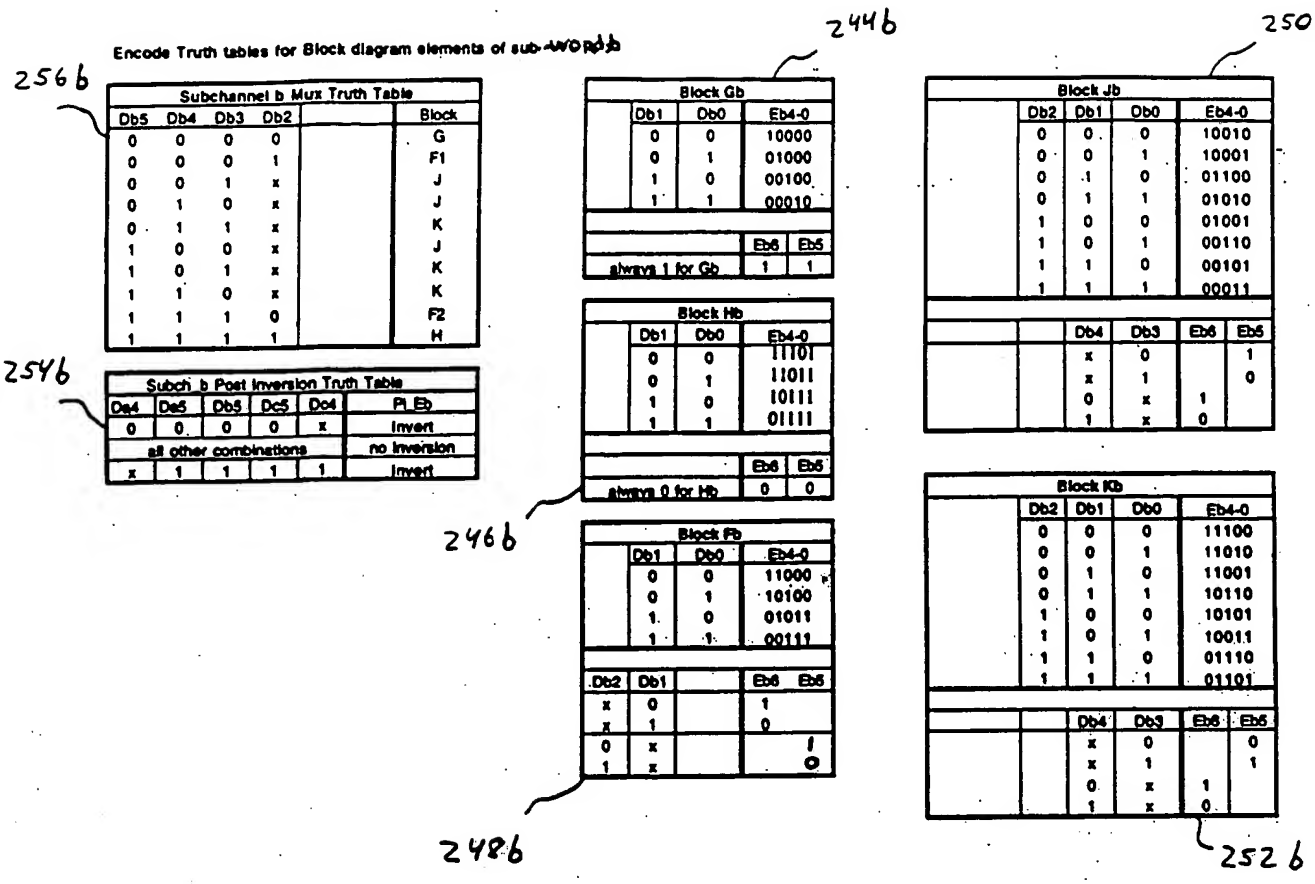

Encode Truth tables for Block diagram elements of sub-WORD b
256b
Subchannel b Mux Truth Table
Db5 Db4 Db3 Db2 Block
0 0 0 0 G
0 0 0 1 F1
0 0 1 x J
0 1 0 x J
0 1 1 x K
1 0 0 x J
1 0 1 x K
1 1 0 x K
1 1 1 0 F2
1 1 1 1 H
254b
Subch b Post Inversion Truth Table
Db4 Db5 Db5 Dc5 Dc4 Pt Eb
0 0 0 0 x Invert
all other combinations no inversion
x 1 1 1 1 Invert
244b
Block Gb
Db1 Db0 Eb4-0
0 0 10000
0 1 01000
1 0 00100
1 1 00010
Eb6 Eb5
always 1 for Gb 1 1
Block Hb
Db1 Db0 Eb4-0
0 0 11101
0 1 11011
1 0 10111
1 1 01111
Eb6 Eb5
always 0 for Hb 0 0
246b
Block Fb
Db1 Db0 Eb4-0
0 0 11000
0 1 10100
1 0 01011
1 1 00111
Db2 Db1 Eb6 Eb5
x 0 1
x 1 0
0 x 1
1 x 0
248b
250b
Block Jb
Db2 Db1 Db0 Eb4-0
0 0 0 10010
0 0 1 10001
0 1 0 01100
0 1 1 01010
1 0 0 01001
1 0 1 00110
1 1 0 00101
1 1 1 00011
Db4 Db3 Eb6 Eb5
x 0 1
x 1 0
0 x 1
1 x 0
Block Kb
Db2 Db1 Db0 Eb4-0
0 0 0 11100
0 0 1 11010
0 1 0 11001
0 1 1 10110
1 0 0 10101
1 0 1 10011
1 1 0 01110
1 1 1 01101
Db4 Db3 Eb6 Eb5
x 0 0
x 1 1
0 x 1
1 x 0
252b

FIG 16

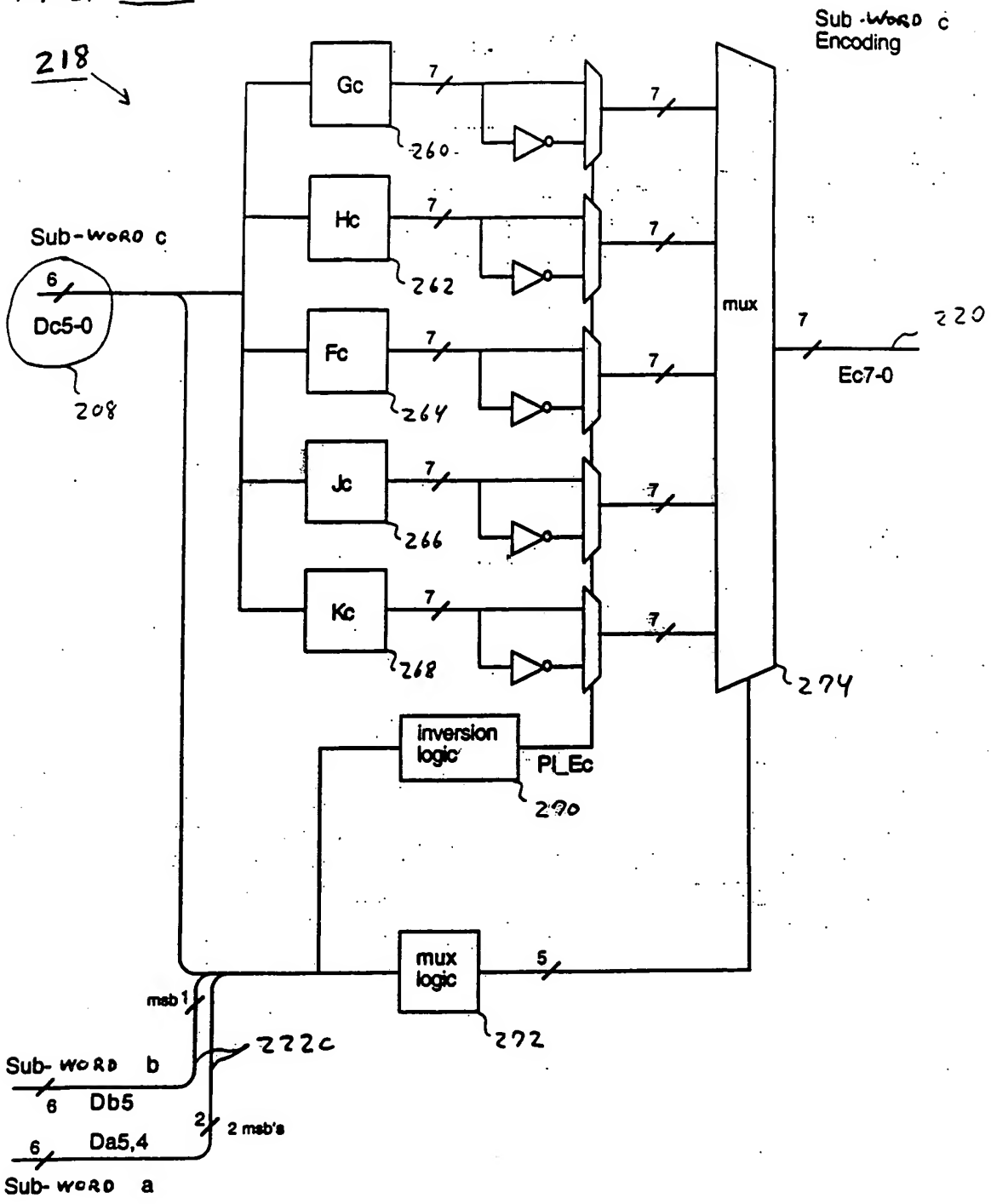

218
Sub-word c Encoding
Gc
Hc
Fc
Jc
Kc
7
260
262
264
266
268
Sub-word c
6
Dc5-0
208
mux
7
220
Ec7-0
274
inversion logic
PI_Ec
270
mux logic
5
272
msb 1
222c
Sub-word b
6
Db5
2
2 msb's
6
Da5,4
Sub-word a

FIG 17

Encode Truth tables for Block diagram elements of sub-word c

Subchannel c Mux Truth Table — 272c

Dc5	Dc4	Dc3	Dc2	Da5·Db5	Block
0	0	0	0	x	G
0	0	0	1	x	F1
0	0	1	x	x	J
0	1	0	x	x	J
0	1	1	x	x	K
1	0	0	x	0	J
1	0	0	x	1	G
1	0	1	x	0	K
1	0	1	x	1	J
1	1	0	x	x	K
1	1	1	0	0	F2
1	1	1	1	0	H
1	1	1	x	1	H

Subch c Post Inversion Truth Table — 270c

Da4+Da5+Db5+Dc5	P1 Ec
0	invert
1	no inversion

Block Gc — 260c

Dc1	Dc0	Ec4-0
0	0	10000
0	1	01000
1	0	00100
1	1	00010

Dc5	Dc2	Ec6	Ec5
0	0	1	1
1	0	0	1
1	1	1	0

Block Hc — 262c

Dc1	Dc0	Ec4-0
0	0	11101
0	1	11011
1	0	10111
1	1	01111

Da5·Db5	Dc2	Ec6	Ec5
0	x	0	0
1	0	0	1
1	1	1	0

Block Fc — 264c

Dc1	Dc0	Ec4-0
0	0	11000
0	1	10100
1	0	01011
1	1	00111

Dc2	Dc1		Ec6	Ec5
x	0		1	
x	1		0	
0	x			1
1	x			0

Block Jc — 266c

Dc2	Dc1	Dc0	Ec4-0
0	0	0	10010
0	0	1	10001
0	1	0	01100
0	1	1	01010
1	0	0	01001
1	0	1	00110
1	1	0	00101
1	1	1	00011

	Dc5		Dc3	Ec6	Ec5
			0		1
			1		0
	0		0	0	
	0		1	1	
	1		0	1	
	1		1	0	

Block Kc — 268c

Dc2	Dc1	Dc0	Ec4-0
0	0	0	11100
0	0	1	11010
0	1	0	11001
0	1	1	10110
1	0	0	10101
1	0	1	10011
1	1	0	01110
1	1	1	01101

Da5·Db5		Dc4	Dc3	Ec6	Ec5
0		x	0		0
0		x	1		1
0		0	x	1	
0		1	x	0	
1		x	x	1	1

FIG 18

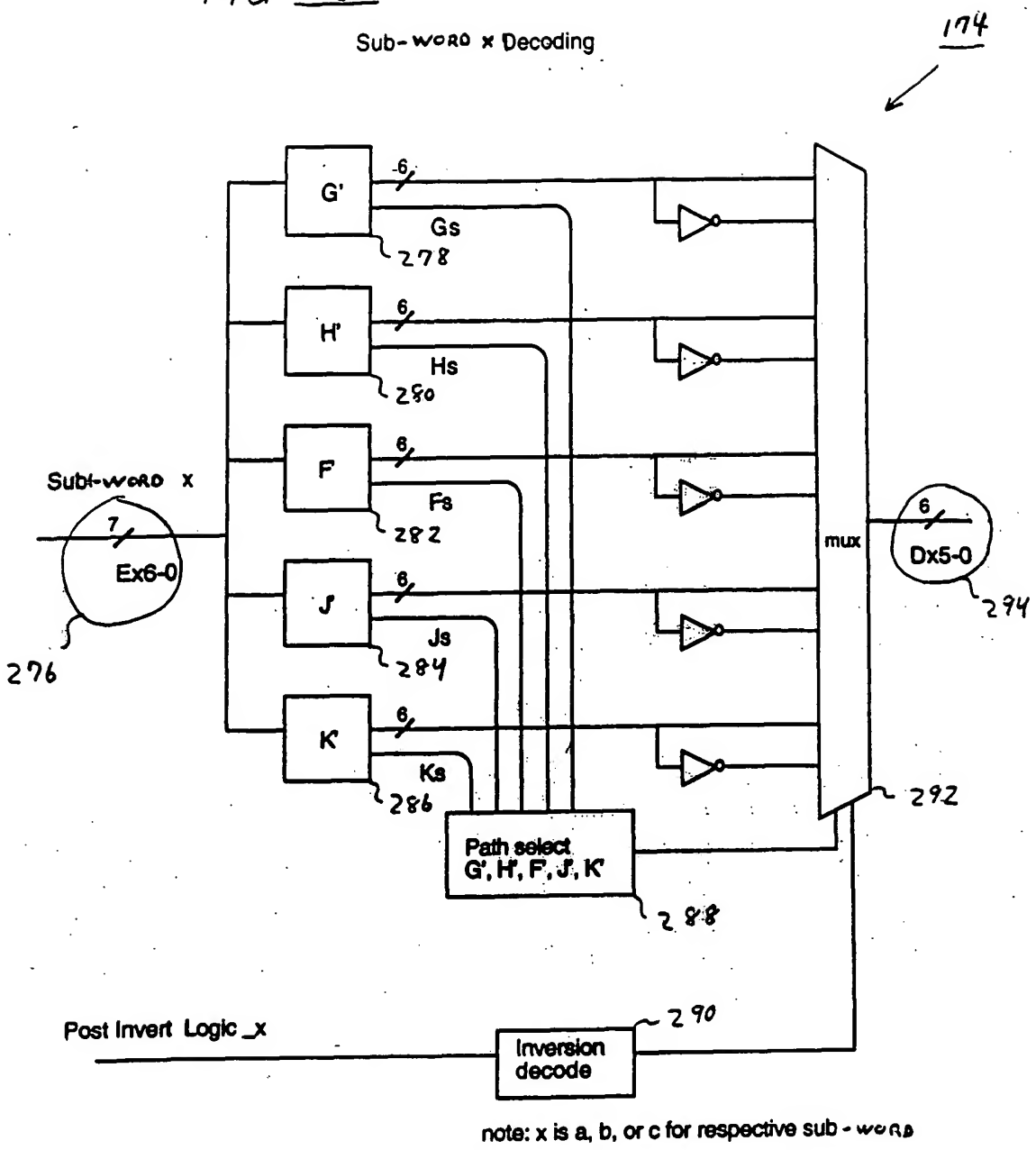

Sub-word x Decoding
174
G'
6
Gs
278
H'
6
Hs
280
F'
6
Fs
282
J'
6
Js
284
K'
6
Ks
286
Sub-word x
7
Ex6-0
276
mux
6
Dx5-0
294
292
Path select
G', H', F', J', K'
288
Post Invert Logic _x
290
Inversion
decode
note: x is a, b, or c for respective sub-word

FIG 19

290

Truth Table for Sub-WordA Decode

Decode Mux Truth Table Sub-Word a

Ea4-0	Decode Path Mux Control Gas	Has	Fas	Jas	Kas	Block	Da5	Da4	Da3	Da2	Da1	Da0	
10000	1	0	0	0	0	G'	0	0	0	Ea5_	0	0	278a
01000	1	0	0	0	0	G'	0	0	0	Ea5_	0	1	
00100	1	0	0	0	0	G'	0	0	0	Ea5_	1	0	
00010	1	0	0	0	0	G'	0	0	0	Ea5_	1	1	
11101	0	1	0	0	0	H'	Ea6_·Ea5_	1	1	Ea5_	0	0	280a
11011	0	1	0	0	0	H'	Ea6_·Ea5_	1	1	Ea5_	0	1	
10111	0	1	0	0	0	H'	Ea6_·Ea5_	1	1	Ea5_	1	0	
01111	0	1	0	0	0	H'	Ea6_·Ea5_	1	1	Ea5_	1	1	
11000	0	0	1	0	0	F'	Ea5	Ea5	Ea5	Ea5_	0	0	282a
10100	0	0	1	0	0	F'	Ea5	Ea5	Ea5	Ea5_	0	1	
01011	0	0	1	0	0	F'	Ea5	Ea5	Ea5	Ea5_	1	0	
00111	0	0	1	0	0	F'	Ea5	Ea5	Ea5	Ea5_	1	1	
10010	0	0	0	1	0	J'	Ea5·Ea6	Ea6_·Ea5	Ea5_	0	0	0	284a
10001	0	0	0	1	0	J'	Ea5·Ea6	Ea6_·Ea5	Ea5_	0	0	1	
01100	0	0	0	1	0	J'	Ea5·Ea6	Ea6_·Ea5	Ea5_	0	1	0	
01010	0	0	0	1	0	J'	Ea5·Ea6	Ea6_·Ea5	Ea5_	0	1	1	
01001	0	0	0	1	0	J'	Ea5·Ea6	Ea6_·Ea5	Ea5_	1	0	0	
00110	0	0	0	1	0	J'	Ea5·Ea6	Ea6_·Ea5	Ea5_	1	0	1	
00101	0	0	0	1	0	J'	Ea5·Ea6	Ea6_·Ea5	Ea5_	1	1	0	
00011	0	0	0	1	0	J'	Ea5·Ea6	Ea6_·Ea5	Ea5_	1	1	1	
11100	0	0	0	0	1	K'	Ea6 xor Ea5	Ea6_ + Ea5	Ea5_	0	0	0	286a
11010	0	0	0	0	1	K'	Ea6 xor Ea5	Ea6_ + Ea5	Ea5_	0	0	1	
11001	0	0	0	0	1	K'	Ea6 xor Ea5	Ea6_ + Ea5	Ea5_	0	1	0	
10110	0	0	0	0	1	K'	Ea6 xor Ea5	Ea6_ + Ea5	Ea5_	0	1	1	
10101	0	0	0	0	1	K'	Ea6 xor Ea5	Ea6_ + Ea5	Ea5_	1	0	0	
10011	0	0	0	0	1	K'	Ea6 xor Ea5	Ea6_ + Ea5	Ea5_	1	0	1	
01110	0	0	0	0	1	K'	Ea6 xor Ea5	Ea6_ + Ea5	Ea5_	1	1	0	
01101	0	0	0	0	1	K'	Ea6 xor Ea5	Ea6_ + Ea5	Ea5_	1	1	1	

Post Inversion Logic

Invert Results of sub-word a decode if WSubCh_c =1

INVERT DECODED VALUE FOR SUB-WORD a IF THE WEIGHT OF SUB-WORD c EQUALS FIVE

290a

FIG 20

298

Decode Mux Truth Table Sub-Word b

Eb4-0	Decode Path Mux Control Gbs	Hbs	Fbs	Jbs	Kbs	Block	Db5	Db4	Db3	Db2	Db1	Db0	
10000	1	0	0	0	0	G′	0	0	0	0	0	0	278b
01000	1	0	0	0	0	G′	0	0	0	0	0	1	
00100	1	0	0	0	0	G′	0	0	0	0	1	0	
00010	1	0	0	0	0	G′	0	0	0	0	1	1	
11101	0	1	0	0	0	H′	1	1	1	1	0	0	280b
11011	0	1	0	0	0	H′	1	1	1	1	0	1	
10111	0	1	0	0	0	H′	1	1	1	1	1	0	
01111	0	1	0	0	0	H′	1	1	1	1	1	1	
11000	0	0	1	0	0	F′	Eb5	Eb5	Eb5	Eb5_	0	0	282b
10100	0	0	1	0	0	F′	Eb5	Eb5	Eb5	Eb5_	0	1	
01011	0	0	1	0	0	F′	Eb5	Eb5	Eb5	Eb5_	1	0	
00111	0	0	1	0	0	F′	Eb5	Eb5	Eb5	Eb5_	1	1	
10010	0	0	0	1	0	J′	Eb5·Eb6	Eb6_	Eb5_	0	0	0	284b
10001	0	0	0	1	0	J′	Eb5·Eb6	Eb6_	Eb5_	0	0	1	
01100	0	0	0	1	0	J′	Eb5·Eb6	Eb6_	Eb5_	0	1	0	
01010	0	0	0	1	0	J′	Eb5·Eb6	Eb6_	Eb5_	0	1	1	
01001	0	0	0	1	0	J′	Eb5·Eb6	Eb6_	Eb5_	1	0	0	
00110	0	0	0	1	0	J′	Eb5·Eb6	Eb6_	Eb5_	1	0	1	
00101	0	0	0	1	0	J′	Eb5·Eb6	Eb6_	Eb5_	1	1	0	
00011	0	0	0	1	0	J′	Eb5·Eb6	Eb6_	Eb5_	1	1	1	
11100	0	0	0	0	1	K′	Eb6 + Eb5	Eb6_	Eb5_	0	0	0	286b
11010	0	0	0	0	1	K′	Eb6 + Eb5	Eb6_	Eb5_	0	0	1	
11001	0	0	0	0	1	K′	Eb6 + Eb5	Eb6_	Eb5_	0	1	0	
10110	0	0	0	0	1	K′	Eb6 + Eb5	Eb6_	Eb5_	0	1	1	
10101	0	0	0	0	1	K′	Eb6 + Eb5	Eb6_	Eb5_	1	0	0	
10011	0	0	0	0	1	K′	Eb6 + Eb5	Eb6_	Eb5_	1	0	1	
01110	0	0	0	0	1	K′	Eb6 + Eb5	Eb6_	Eb5_	1	1	0	
01101	0	0	0	0	1	K′	Eb6 + Eb5	Eb6_	Eb5_	1	1	1	

Post Inversion Logic

Invert Results of sub-word _b decode if W5subCh_c + W2subCh_a =1
W5subCh_c = Kcs·Ec6·Ec5 + Hcs·(Ec6 + Ec5)
W2subCh_a = Jas·Ea6_·Ea5_ + Gas·(Ea6_ + Ea5_)

INVERT DECODED VALUE FOR SUB-WORD b IF THE WEIGHT OF SUB-WORD c = 5 , AND OR THE WEIGHT OF SUB-WORD a = 2

290 b

FIG 21

300

Decode Mux Truth Table Sub WORD c

Ec4-0	Decode Path Mux Control Gcs	Hcs	Fcs	Jcs	Kcs	Block	Dc5	Dc4	Dc3	Dc2	Dc1	Dc0	
10000	1	0	0	0	0	G'	Ec6_+Ec5_	0	0	Ec5_	0	0	278c
01000	1	0	0	0	0	G'	Ec6_+Ec5_	0	0	Ec5_	0	1	
00100	1	0	0	0	0	G'	Ec6_+Ec5_	0	0	Ec5_	1	0	
00010	1	0	0	0	0	G'	Ec6_+Ec5_	0	0	Ec5_	1	1	
11101	0	1	0	0	0	H'	1	1	1	Ec5_	0	0	280c
11011	0	1	0	0	0	H'	1	1	1	Ec5_	0	1	
10111	0	1	0	0	0	H'	1	1	1	Ec5_	1	0	
01111	0	1	0	0	0	H'	1	1	1	Ec5_	1	1	
11000	0	0	1	0	0	F'	Ec5	Ec5	Ec5	Ec5_	0	0	282c
10100	0	0	1	0	0	F'	Ec5	Ec5	Ec5	Ec5_	0	1	
01011	0	0	1	0	0	F'	Ec5	Ec5	Ec5	Ec5_	1	0	
00111	0	0	1	0	0	F'	Ec5	Ec5	Ec5	Ec5_	1	1	
10010	0	0	0	1	0	J'	(Ec5 xor Ec6)_	Ec6_ · Ec5	Ec5_	0	0	0	284c
10001	0	0	0	1	0	J'	(Ec5 xor Ec6)_	Ec6_ · Ec5	Ec5_	0	0	1	
01100	0	0	0	1	0	J'	(Ec5 xor Ec6)_	Ec6_ · Ec5	Ec5_	0	1	0	
01010	0	0	0	1	0	J'	(Ec5 xor Ec6)_	Ec6_ · Ec5	Ec5_	0	1	1	
01001	0	0	0	1	0	J'	(Ec5 xor Ec6)_	Ec6_ · Ec5	Ec5_	1	0	0	
00110	0	0	0	1	0	J'	(Ec5 xor Ec6)_	Ec6_ · Ec5	Ec5_	1	0	1	
00101	0	0	0	1	0	J'	(Ec5 xor Ec6)_	Ec6_ · Ec5	Ec5_	1	1	0	
00011	0	0	0	1	0	J'	(Ec5 xor Ec6)_	Ec6_ · Ec5	Ec5_	1	1	1	
11100	0	0	0	0	1	K'	Ec6 + Ec5	Ec6_ + Ec5	Ec5_	0	0	0	286c
11010	0	0	0	0	1	K'	Ec6 + Ec5	Ec6_ + Ec5	Ec5_	0	0	1	
11001	0	0	0	0	1	K'	Ec6 + Ec5	Ec6_ + Ec5	Ec5_	0	1	0	
10110	0	0	0	0	1	K'	Ec6 + Ec5	Ec6_ + Ec5	Ec5_	0	1	1	
10101	0	0	0	0	1	K'	Ec6 + Ec5	Ec6_ + Ec5	Ec5_	1	0	0	
10011	0	0	0	0	1	K'	Ec6 + Ec5	Ec6_ + Ec5	Ec5_	1	0	1	
01110	0	0	0	0	1	K'	Ec6 + Ec5	Ec6_ + Ec5	Ec5_	1	1	0	
01101	0	0	0	0	1	K'	Ec6 + Ec5	Ec6_ + Ec5	Ec5_	1	1	1	

Post Inversion Logic

Invert Results of sub-word b decode if W2subCh_a =1

W2subCh_a = Jas·Ea6_·Ea5_ + Gas·(Ea6_ + Ea5_)

INVERT DECODED VALUE FOR SUB-WORD C IF THE WEIGHT OF SUB-WORD a = 2

290c

FIGURE 22

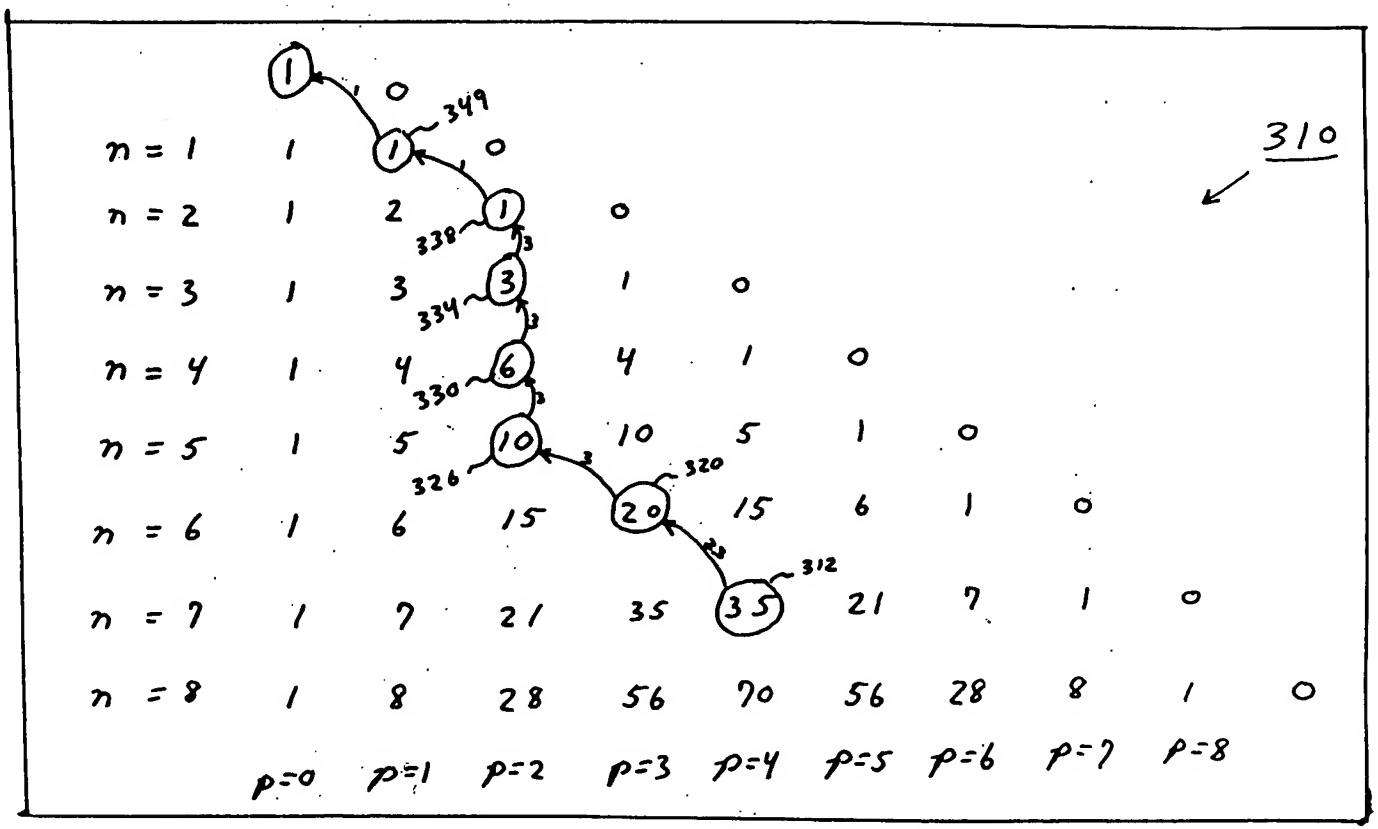
(4B / 6L EXAMPLE)

CORRESPONDANCE BETWEEN DECIMAL, BINARY, AND ENCODED VALUES

302

304 DECIMAL VALUE	306 BINARY VALUE	308 ENCODED VALUE
Decimal Count	Binary Count	Binomial Count
0	0000	000111
1	0001	001011
2	0010	001101
3	0011	001110
4	0100	010011
5	0101	010101
6	0110	010110
7	0111	011001
8	1000	011010
9	1001	011100
10	1010	100011
11	1011	100101
12	1100	100110
13	1101	101001
14	1110	101010
15	1111	101100
16	extra	110001
17	extra	110010
18	extra	110100
19	extra	111000

FIGURE 23



$$n_p = \frac{(n(n-1)(n-2)\ldots n-[p-1])}{1\cdot 2\cdot 3\ldots p}$$ 310a

$58_{10} = 11000110$ 310b

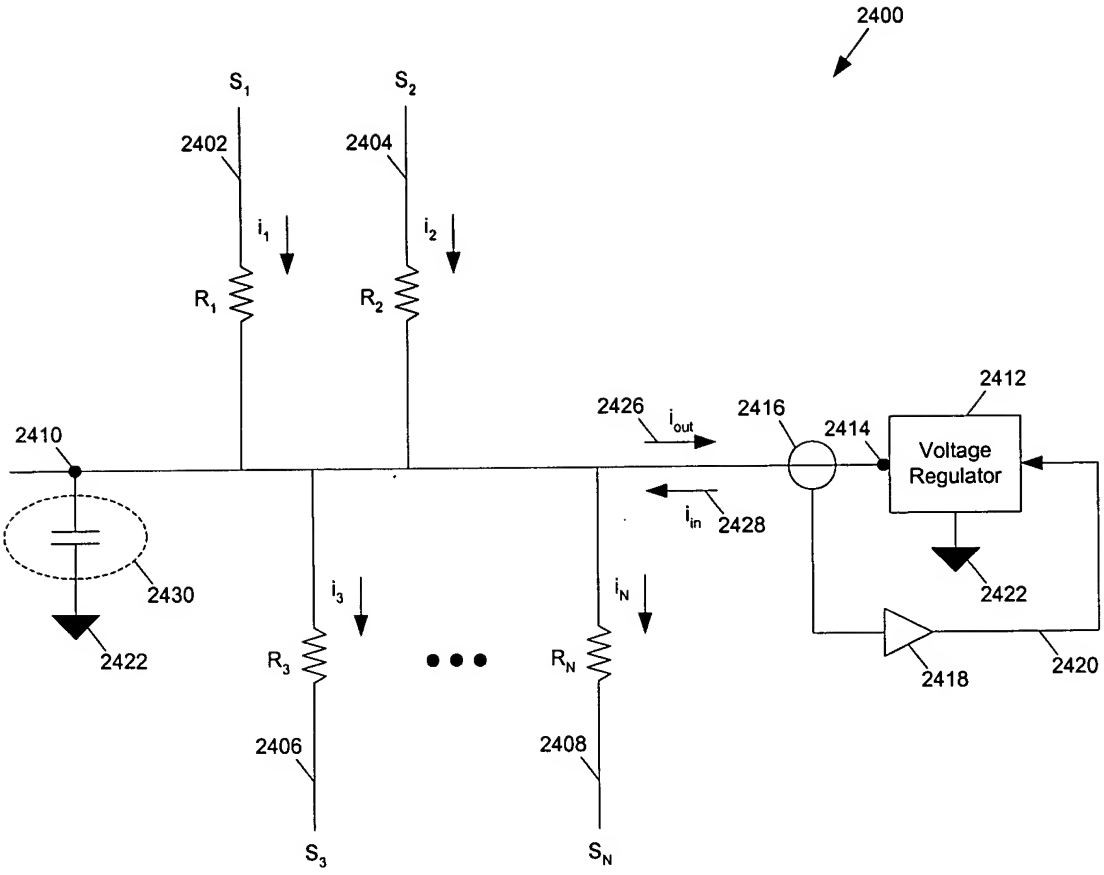

2400
S1
S2
2402
2404
i1
i2
R1
R2
2426
iout
2416
2414
2412
Voltage Regulator
2410
iin
2428
2430
i3
iN
2422
2422
R3
RN
2418
2420
2406
2408
S3
SN

Figure 24

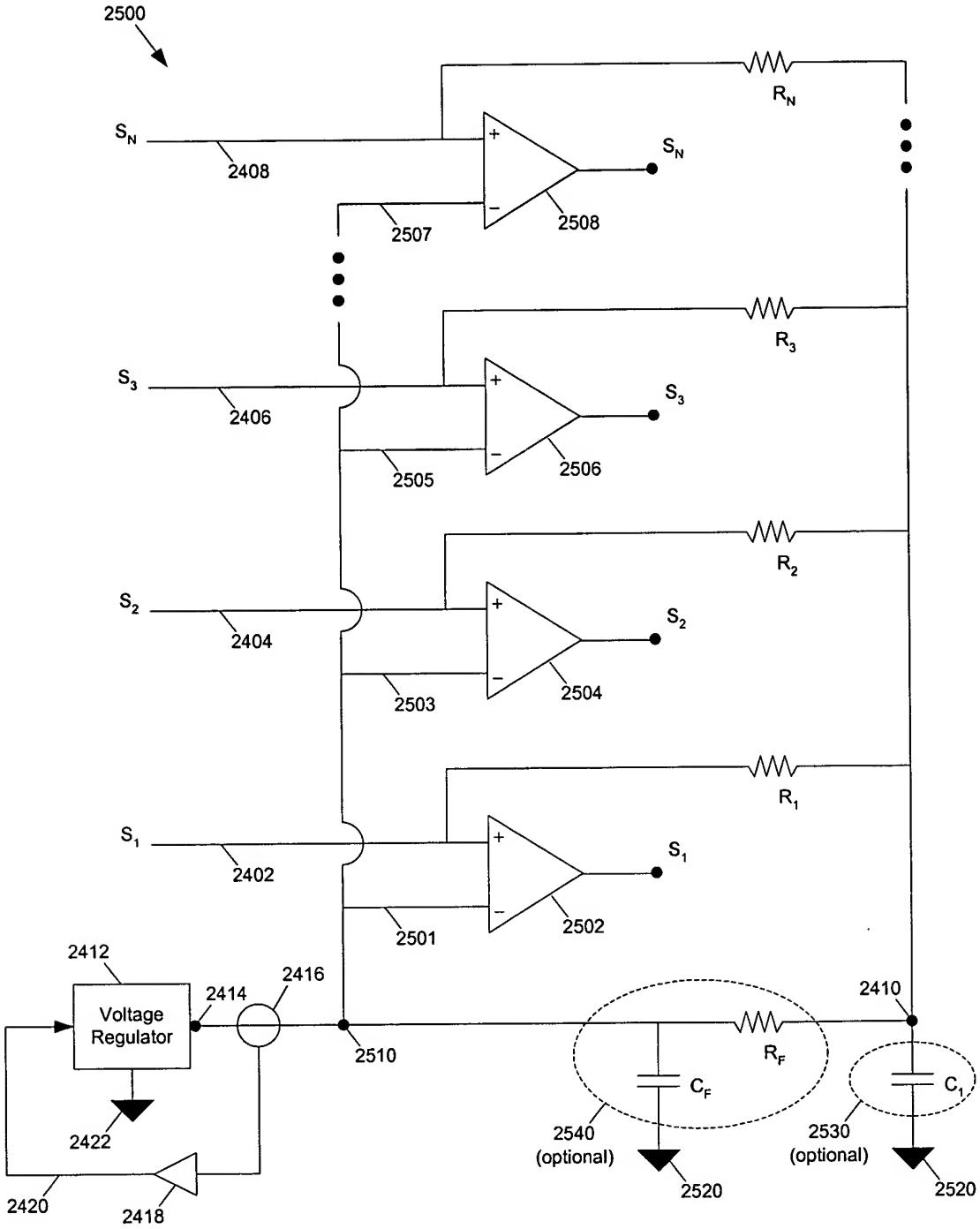

2500
R_N
S_N
2408
S_N
2507
2508
R_3
S_3
2406
S_3
2505
2506
R_2
S_2
2404
S_2
2503
2504
R_1
S_1
2402
S_1
2501
2502
2412
Voltage Regulator
2414
2416
2510
2410
R_F
C_F
C_1
2540 (optional)
2530 (optional)
2520
2520
2422
2420
2418

Figure 25

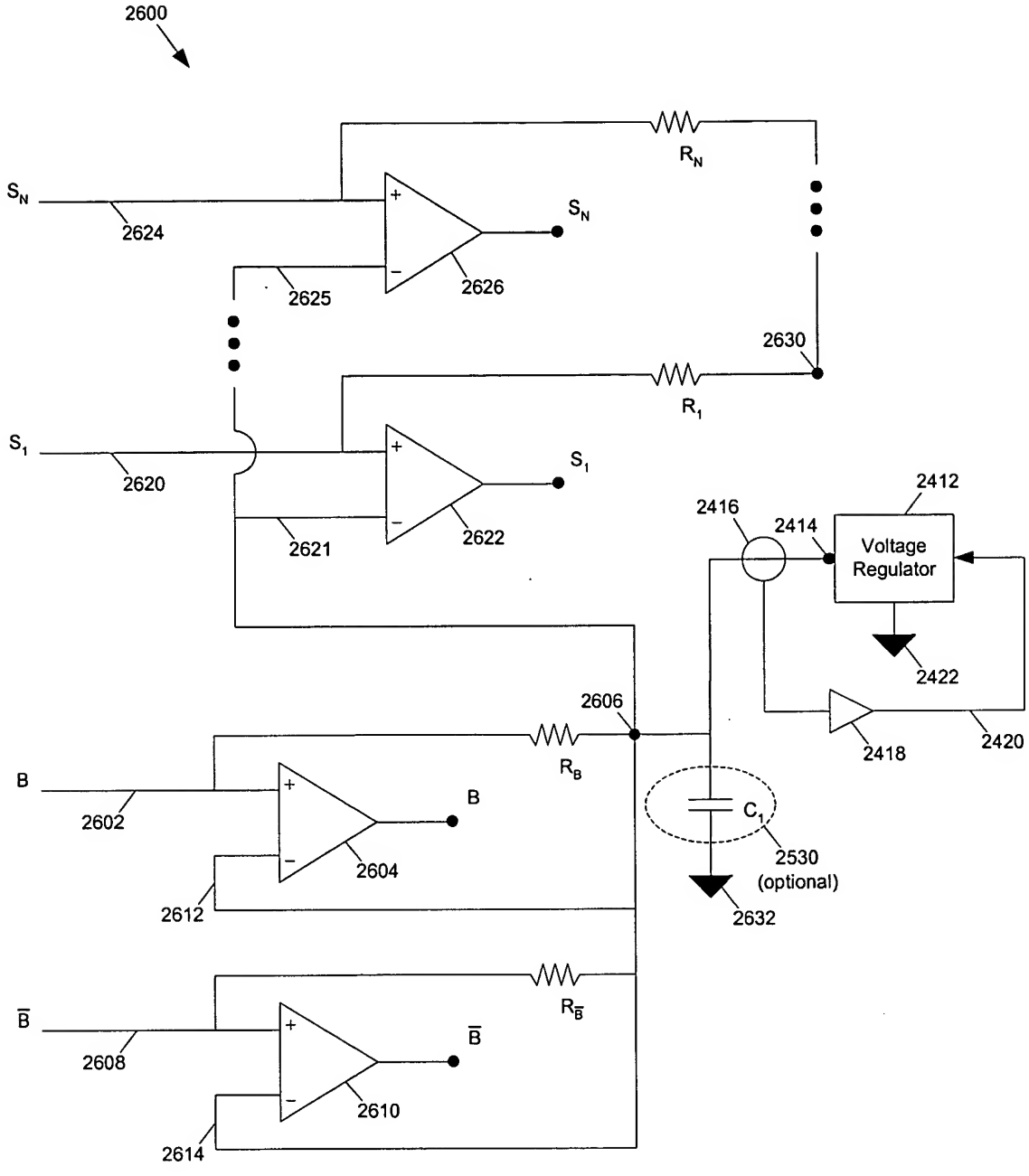

2600
R_N
S_N
2624
S_N
2625
2626
2630
R_1
S_1
2620
S_1
2621
2622
2412
2416
2414
Voltage Regulator
2422
2606
2418
2420
R_B
B
2602
B
2604
2612
C_1
2530
(optional)
2632
$R_{\overline{B}}$
$\overline{B}$
2608
$\overline{B}$
2610
2614

Figure 26

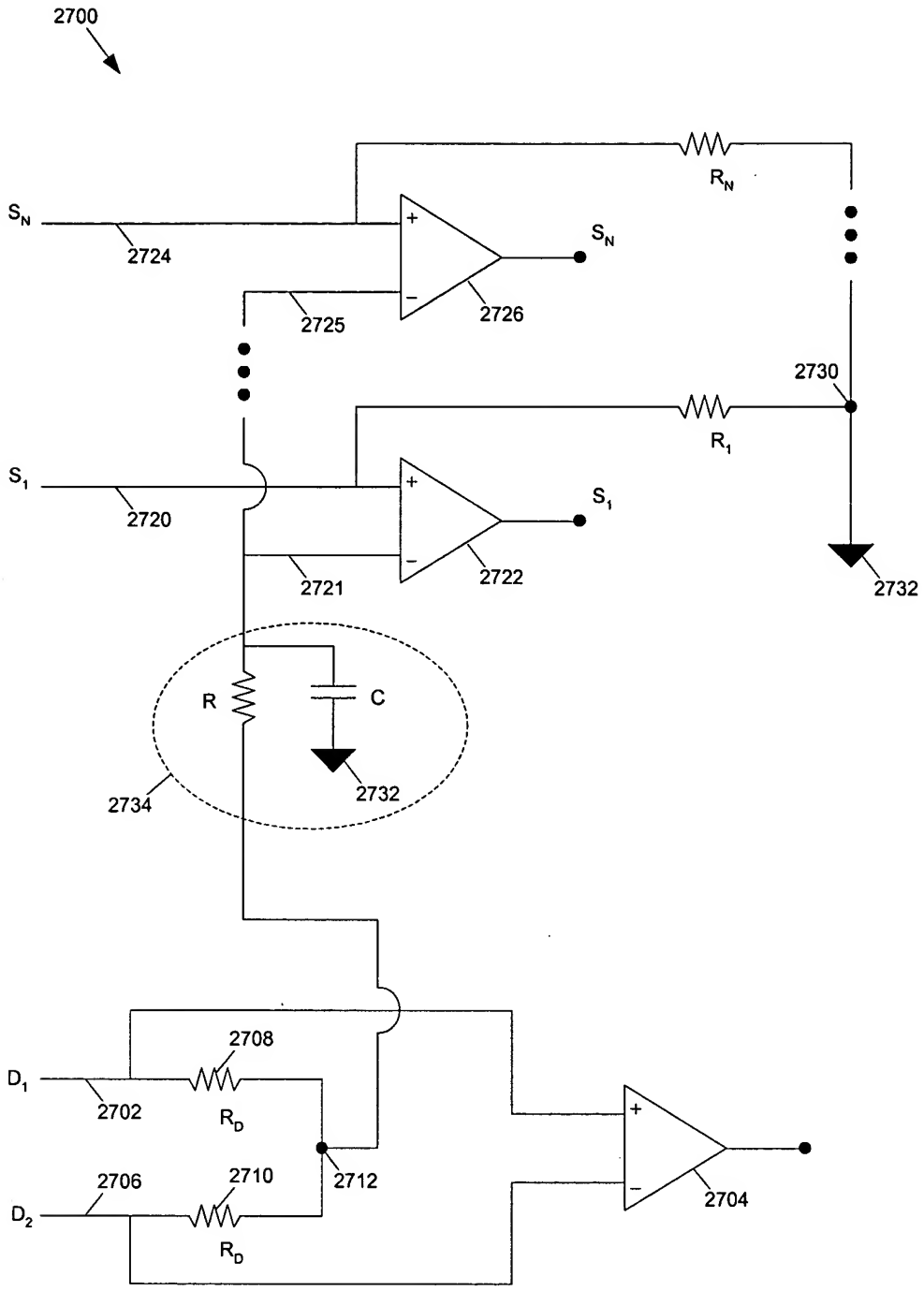

2700
R_N
S_N
2724
S_N
2725
2726
2730
R_1
S_1
2720
S_1
2721
2722
2732
R
C
2734
2732
2708
D_1
2702
R_D
2706
2710
2712
D_2
R_D
2704

Figure 27

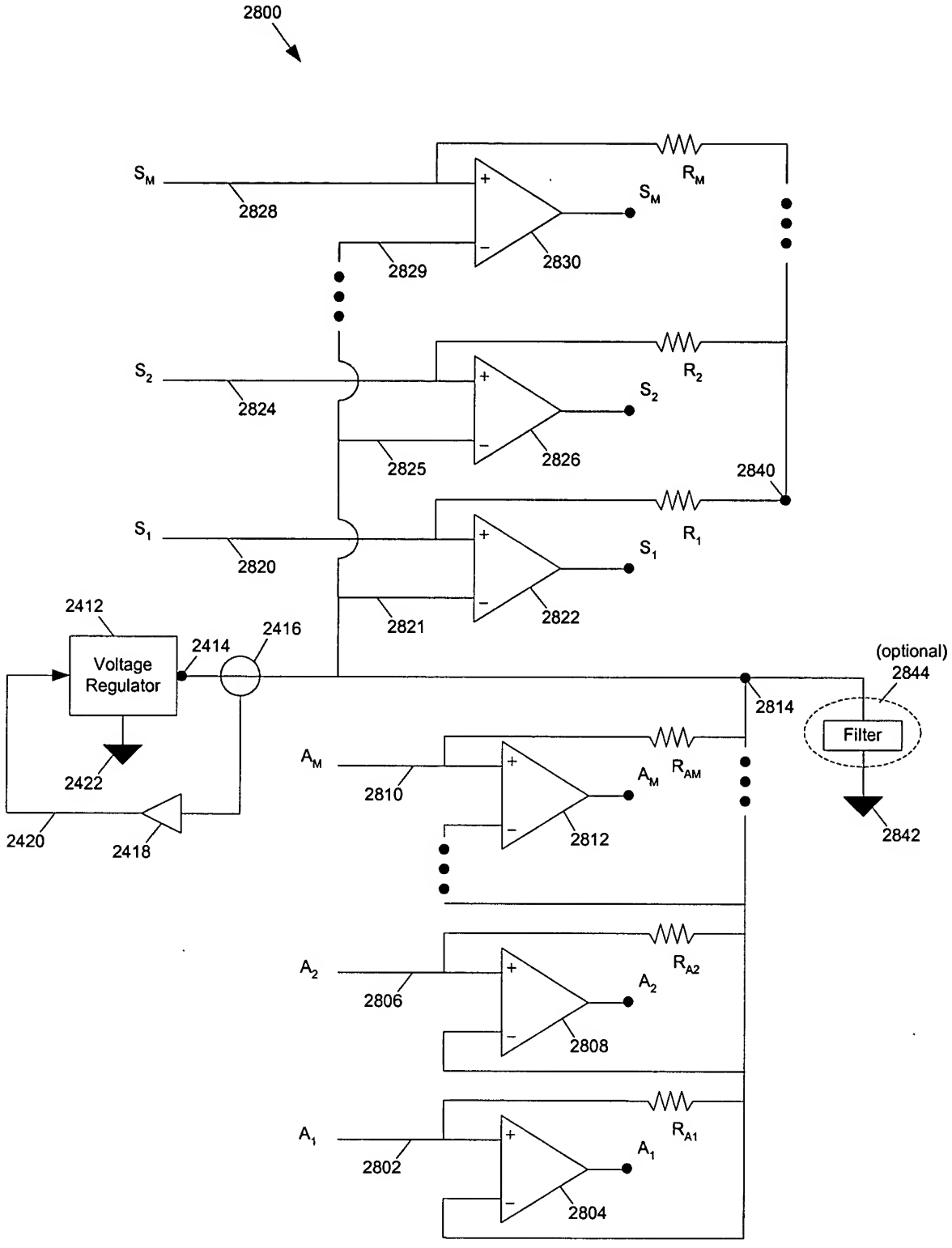

2800
S_M
2828
2829
2830
S_M
R_M
S_2
2824
2825
2826
S_2
R_2
2840
S_1
2820
2821
2822
S_1
R_1
2412
Voltage Regulator
2414
2416
2422
2420
2418
2814
(optional)
2844
Filter
2842
A_M
2810
2812
A_M
R_{AM}
A_2
2806
2808
A_2
R_{A2}
A_1
2802
2804
A_1
R_{A1}

Figure 28